Presentation On 8086 MICROPROCESSOR ARCHITECTURE

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History of 8086 microprocessor

- The 8086 is a 16-bit microprocessor chip designed by Intel between early 1976 and mid-1978.
- The Intel 8088, released in 1979.
- The processor used in the original

  IBM PC.

- The 8086 gave rise to the x86 architecture Intel's most successful processors.

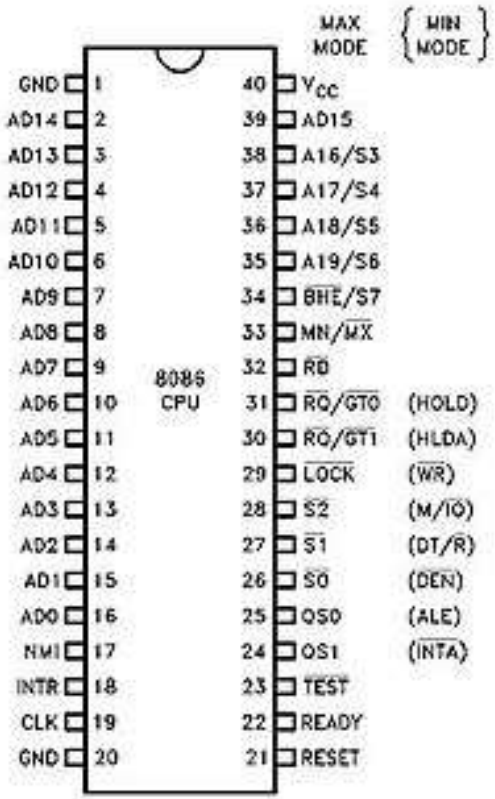
Features of Intel – 8086 microprocessor

- ***It is a 16-bit* microprocessor.**
- ***8086 has a 20 bit address bus can***

  access up to 2^{20} memory locations (1 MB).
- ***It can support up to 64K I/O ports.***
- ***It provides 16 -bit registers***
- ***It has multiplexed address and data bus AD0- AD15 and A16 – A19.***

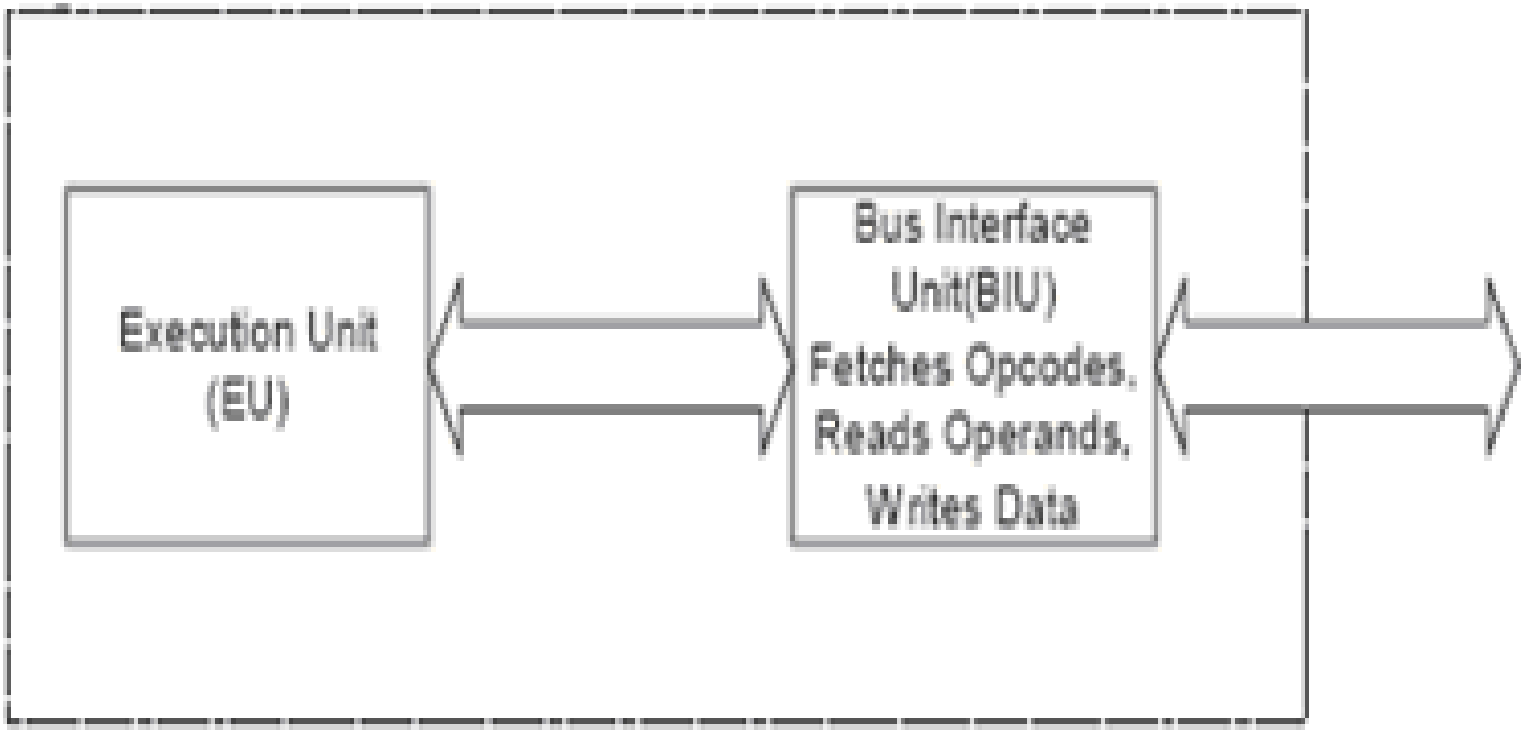
Features of Intel – 8086 microprocessor

- ***8086 is designed to operate in two modes***
  --- Minimum and Maximum
- ***A 40 pin dual in line package***
- ***Address ranges from 00000H to FFFFFH***
- ***It requires +5V power supply.***



Internal Architecture of 8086

- The 8086 CPU logic has been partitioned into two functional units namely Bus Interface Unit (BIU) and Execution Unit (EU)



Internal Architecture of 8086

- **The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory**

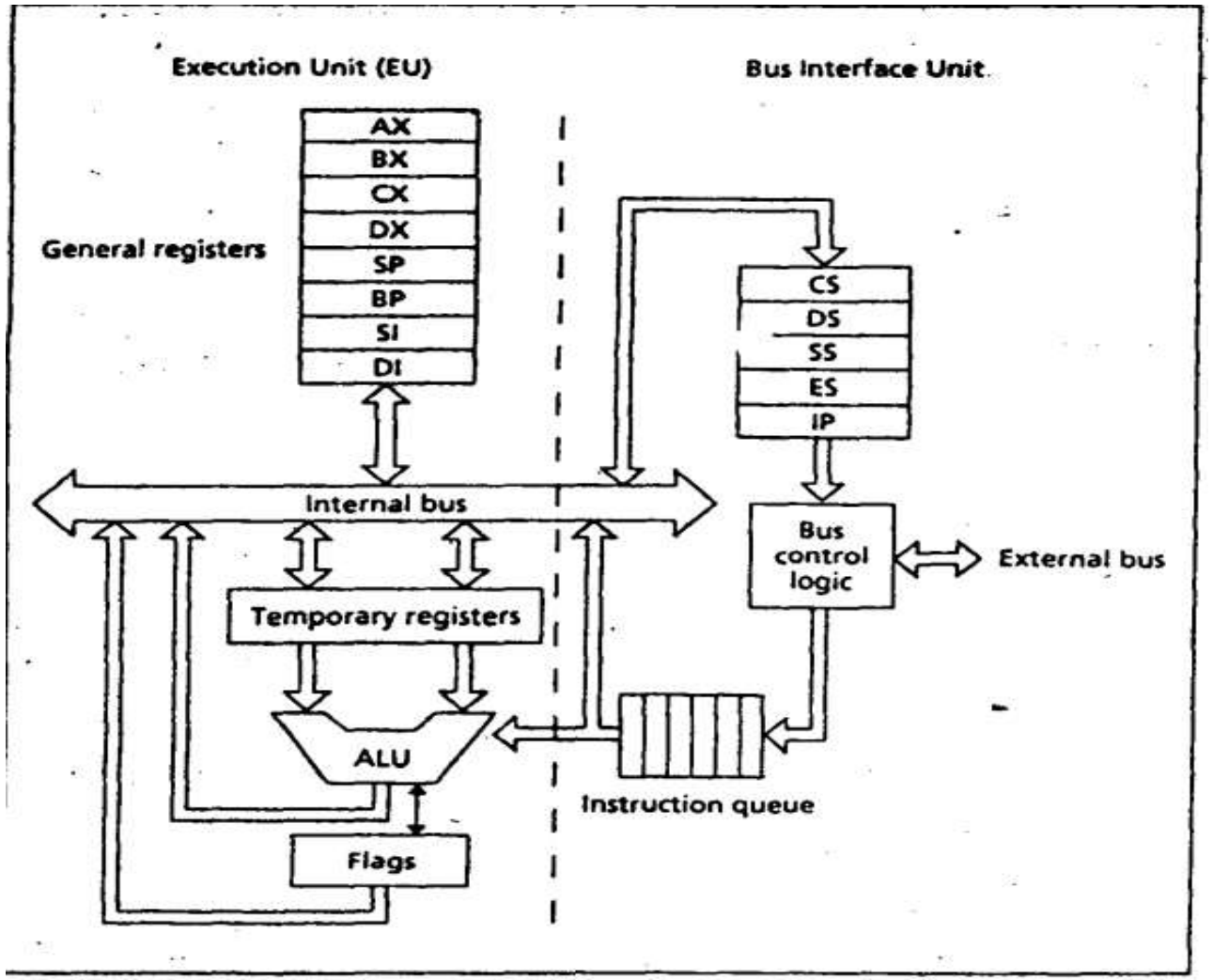
- **EU executes instructions from the instruction system byte queue**

- **The BIU contains a dedicated adder, which is used to produce the 20-bit address.**

Internal Architecture of 8086

The BIU handles all transactions of data and addresses on the buses for EU

The major reason for this separation is to increase the processing speed of the processor

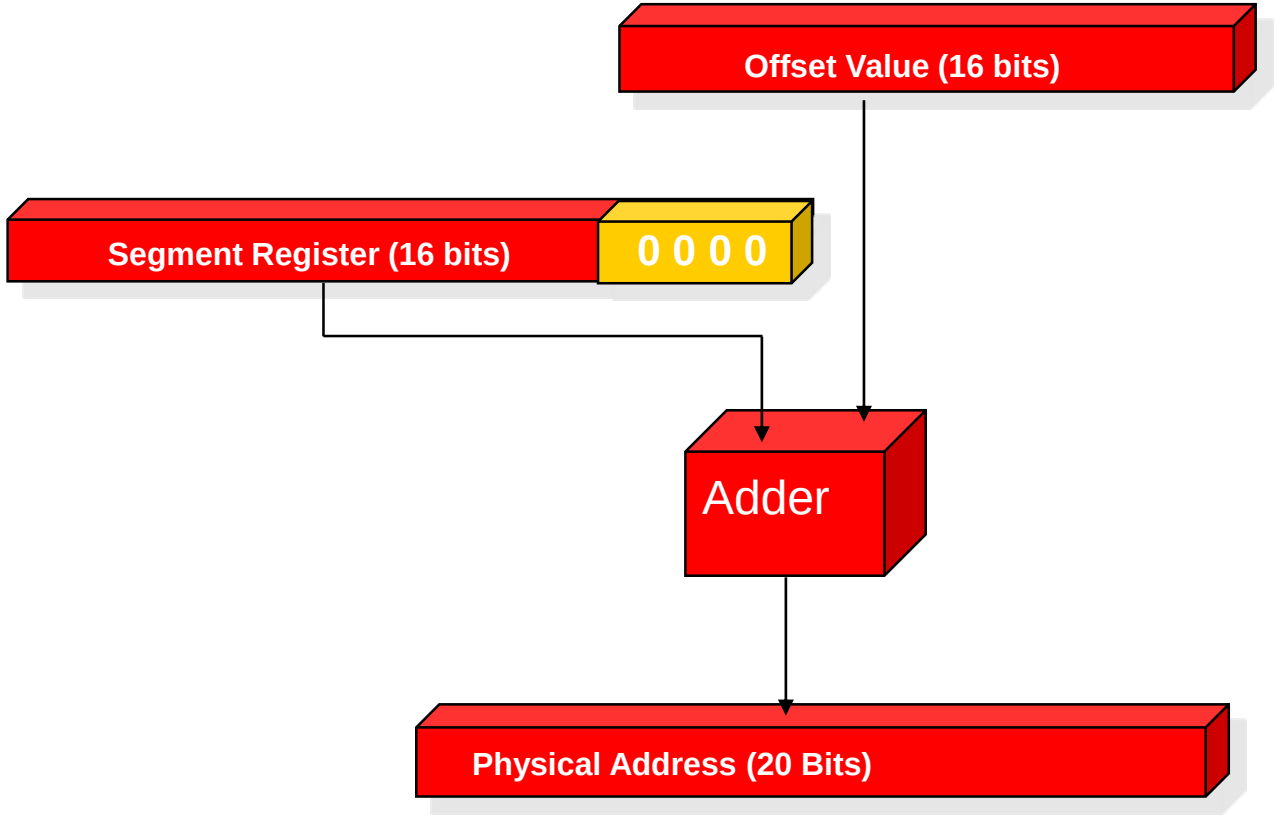


20-bit physical address

1.Programmer-provided logical address(16-bit contents of CS and IP) by logically shifting the contents of CS four bits to left and then adding the 16-bit contents of IP.

2.For example, if [CS] = (456A)16 and [IP] = (1620)16, then the 20-bit physical address is generated by the BIU as follows:
Four times logically shifted [CS] to left = (456A0) 16
+ [IP] as offset = (1620)16
20-bit physical address = (46CC0)16

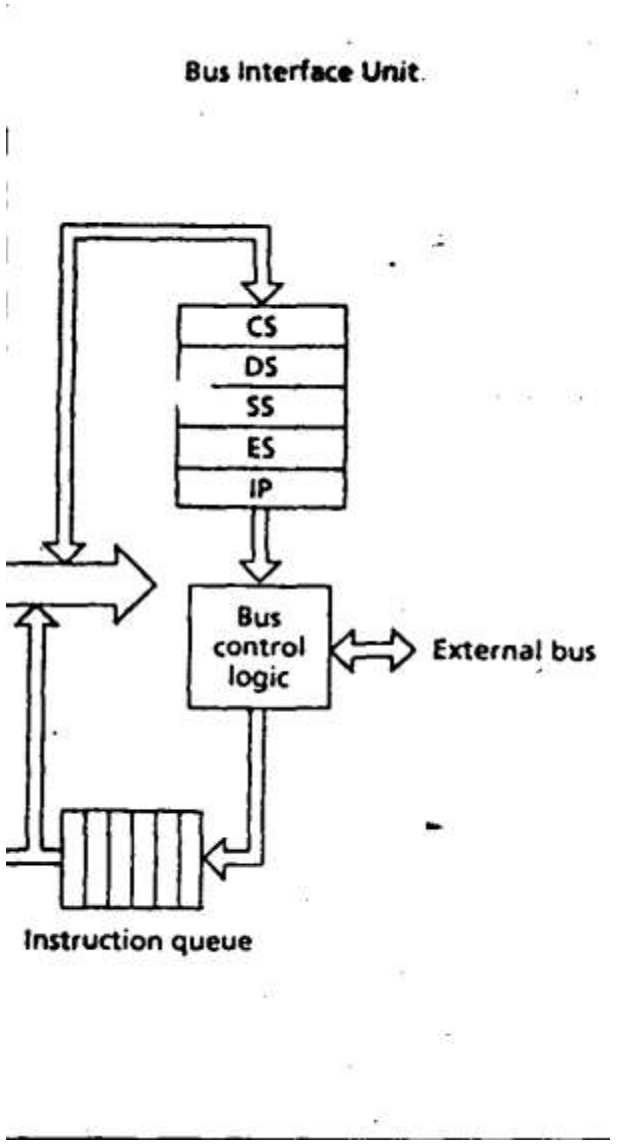
20-bit physical address



Physical address= segment x 1Oh+ offset

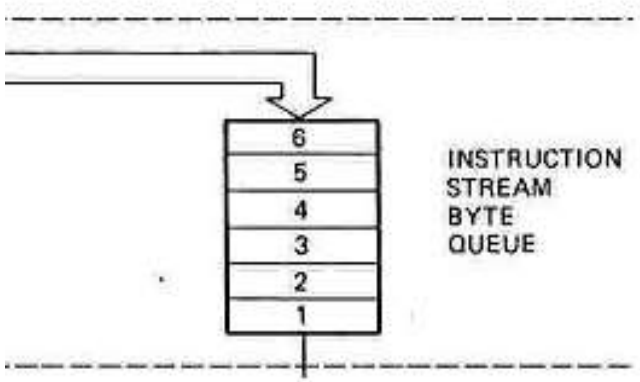
Bus Interface Unit

- The BIU has
  - Instruction stream byte queue
  - A set of segment registers
  - Instruction pointer



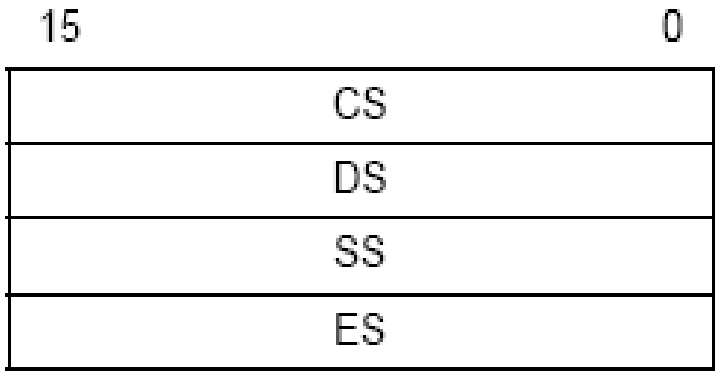
BIU – Instruction Byte Queue

- 8086 instructions vary from 1 to 6 bytes
- Therefore fetch and execution are taking place concurrently in order to improve the performance of the microprocessor
- The BIU feeds the instruction stream to the execution unit through a 6 byte prefetch queue



Segment Registers

- **CS - points at the segment containing the current program.**
- **DS - generally points at segment where variables are defined.**
- **ES - extra segment register, it's up to a coder to define its usage.**
- **SS - points at the segment containing the stack.**

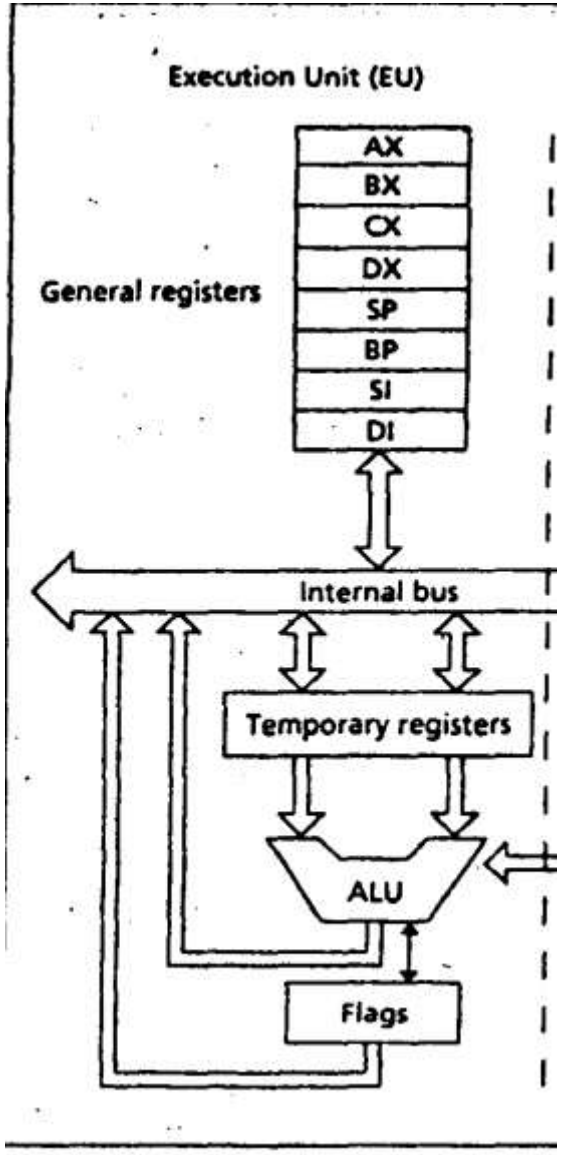


Instruction pointer

- **IP - the instruction pointer:**
  1. Always points to next instruction to be executed
  2. Offset address relative to CS
- **IP register always works together with CS segment register and it points to currently executing instruction.**

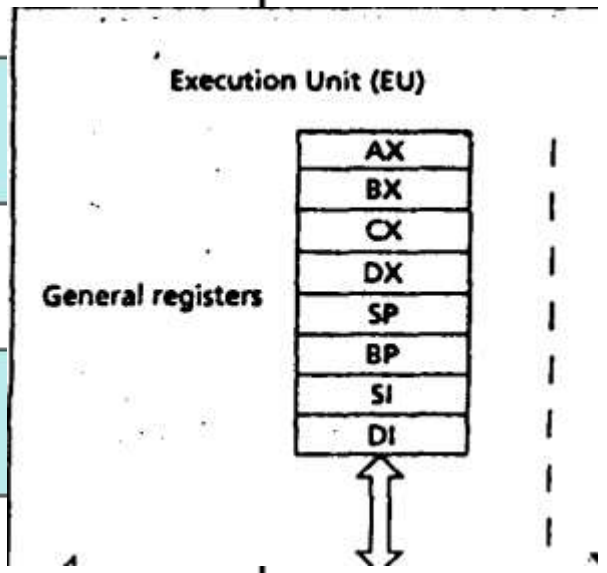
Execution Unit

- General registers
- Arithmetic and Logical Unit (ALU)
- Flag register



General registers

Register	Purpose
AX	Word multiply, word divide, word I /O
AL	Byte multiply, byte divide, byte I/O, decimal arithmetic
AH	Byte multiply, byte divide
BX	Store address information
CX	String operation, loops
CL	Variable shift and rotate
DX	Word multiply, word divide, indirect I/O (Used to hold I/O address during I/O instructions. If the result is more than 16-bits, the lower order 16-bits are stored in accumulator and higher order 16-bits are stored in DX register)



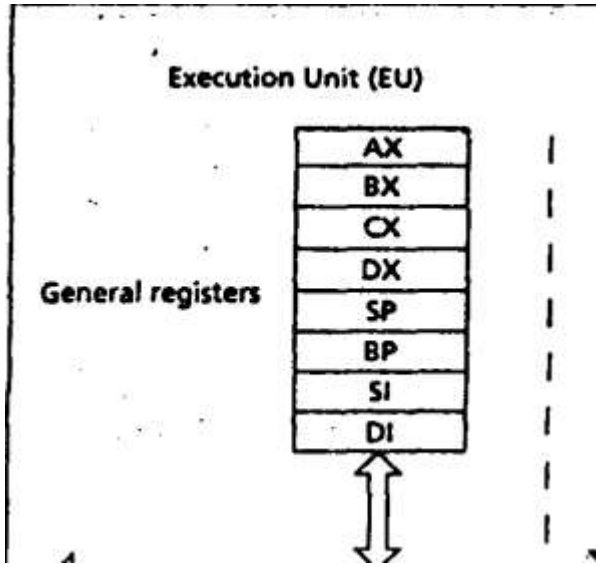
General registers

SI - source index register:
1. Can be used for pointer addressing of data
2. Used as source in some string processing instructions

DI - destination index register:
1. Can be used for pointer addressing of data
2. Used as destination in some string processing instructions

BP - base pointer:
1. Primarily used to access parameters passed via the stack
2. Offset address relative to SS

SP - stack pointer:
1. Always points to top item on the stack
2. Offset address relative to SS



Flag register

Bit Mnemonic	Bit Name	Reset State	Function
OF	Overflow Flag	0	If OF is set, an arithmetic overflow has occurred.
DF	Direction Flag	0	If DF is set, string instructions are processed high address to low address. If DF is clear, strings are processed low address to high address.
IF	Interrupt Enable Flag	0	If IF is set, the CPU recognizes maskable interrupt requests. If IF is clear, maskable interrupts are ignored.
TF	Trap Flag	0	If TF is set, the processor enters single-step mode.
SF	Sign Flag	0	If SF is set, the high-order bit of the result of an operation is 1, indicating it is negative.
ZF	Zero Flag	0	If ZF is set, the result of an operation is zero.
AF	Auxiliary Flag	0	If AF is set, there has been a carry from the low nibble to the high or a borrow from the high nibble to the low nibble of an 8-bit quantity. Used in BCD operations.
PF	Parity Flag	0	If PF is set, the result of an operation has even parity.
CF	Carry Flag	0	If CF is set, there has been a carry out of, or a borrow into, the high-order bit of the result of an instruction.

Arithmetic and Logical Unit

- An arithmetic logic unit (ALU) represents the fundamental building block of the central processing unit of a computer. An ALU is a digital circuit used to perform arithmetic and logic operations.